**AudioADC Module Description Document**

**1.Introduction**

The Audio ADC module supports up to 7 different analog audio source inputs, each with an independent volume control module. The Audio ADC module internally consists of two parts: PGA analog input and analog-to-digital converter (ADC). Among them, the PGA analog input section is used to switch, adjust the volume and mix multiple input audio sources. The analog-to-digital converter (ADC) is a dual-channel path based on a 16-bit high signal-to-noise ratio design. Ultimately, the Audio ADC converts the collected data into digital sampling values, which can not only be written into the Memory but also directly into the I2S module.

In addition, there are two modes for the clock source of the Audio ADC module. One is generated by the internal clock generator, and the other is injected by the external clock through GPIO. Among them, the internal clock generator can produce two types of clocks. One is a clock with an integer multiple sampling rate and an output of 11.2896/12.288MHz. The AP80 is named NORMAL MODE. Another type is not affected by the sampling rate and has a fixed output clock of 12MHz. The AP80 is named USB MODE.

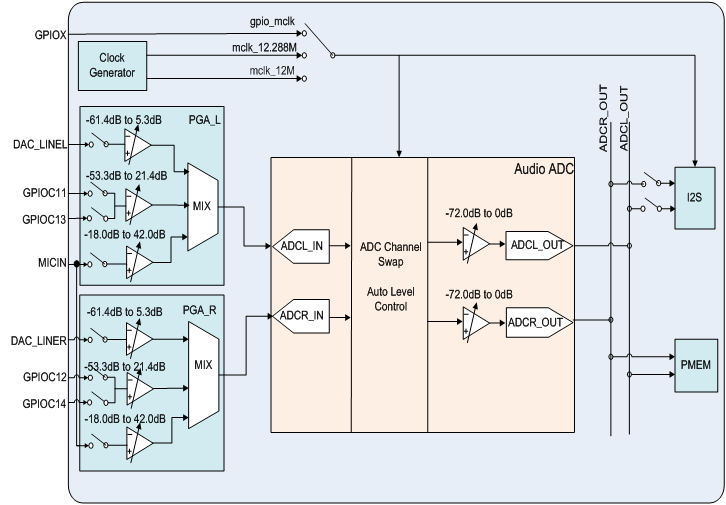


Figure 1 Audio ADC Overall Block Diagram

**2.Main Features**

* Supports up to 7 different analog audio input sources with independent volume control.
* Supports 1 microphone input.
* Input signal amplitude requirement: ≤900 mVrms (equivalent to 2.54 Vp-p).
* Supports digital gain adjustment for sampled values.
* Supports ALC (Automatic Level Control).
* Supports writing digital sample values to PMEM memory.
* Supports outputting digital sample values to the I2S interface.
* Supports left-right channel swapping for digital sample values.
* Supports 9 sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz.
* Supports fine-tuning of the sampling rate.

1. **Function Description**

**3.1 Analog Input**

The Audio ADC module supports up to 7 different analog audio source inputs, including 1 mono MIC path, 1 high-quality dual-channel DAC\_LINEL and DAC\_LINER paths (SNR≥90dB), and 2 dual-channel paths filled through the analog end of GPIO.

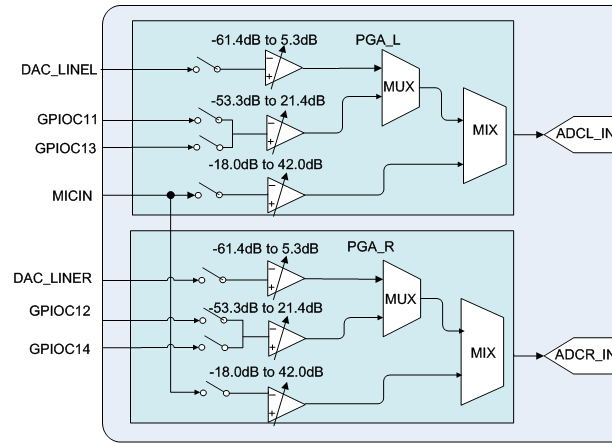


Figure 3 Analog Input Block Diagram

As can be seen from Figure 2, there are three types of input audio sources for PGA: DAC\_LINE/GPIO/MIC. Among them, the DAC\_LINE channel has the functions of high voltage resistance and high signal-to-noise ratio, and the adjustable volume range is -61.4 to 5.3dB. The GPIO channel injects audio signals through the GPIO analog input terminal, with a volume adjustment range of -53.3 to 21.4dB. The MIC pathway is different from other pathways. Its left and right channels have exactly the same mono data. The MIC channel can be mixed with any other channel, but no other channels can be mixed. In addition, the MIC can also enable or disable the bias voltage function.

Table 1 Relevant functions for the PGA mode input terminal

|  |  |
| --- | --- |
| Function name | Description |
| CodecAdcAnaInit | Initialize or deinitialize the relevant functions |
| CodecAdcAnaDeInit |
| CodecAdcChannelSel | 2. Analog Input Source Selection for the PGA |
| CodecAdcMicGainConfig | 3. Volume control functions for each channel, where Fm corresponds to the type of audio source being injected from GPIO |
| CodecAdcLineInGainConfig |
| CodecAdcFmGainConfig |

Additionally, when adjusting the analog input volume, ensure that the signal is conditioned to an appropriate voltage level and does not exceed the maximum input amplitude allowed by the analog-to-digital converter (900 mV RMS). Signals exceeding this maximum input amplitude will result in clipping distortion in the sampled values. This requires special attention when designing and adjusting both the off-chip circuitry of each analog audio path and the on-chip PGA gain.

**3.2 Analog-to-Digital Converter (ADC)**

The Audio ADC module contains a set of dual-channel analog-to-digital converters (ADC), which are used to convert the analog signals output by the PGA into digital signals and then feed them into the subsequent digital circuits. As shown in Figure 3, the ADC module supports left and right channel switching, ALC, and separate control of left and right volume.

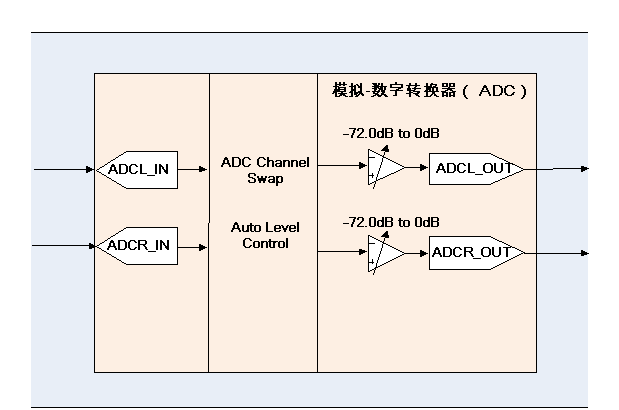


Figure 4 Analog-to-Digital Converter (ADC) Block Diagram

Translation:

模拟-数字转换器(ADC) = Analog-to-Digital Converter (ADC)

**3.2.1 Volume Control**

The left and right channels of the analog-to-digital converter (ADC) can independently control the volume, with a control range of 0dB to -72dB for both. The calculation formula is as follows: when x = 0xfff, the volume of y decreases by 0dB. When x = 1, the volume of y decays by approximately -72dB.

IMG_256 (Formula 1)

Table 2 Related functions for volume control of analog-to-digital converters

|  |  |
| --- | --- |
| Function name | Description |
| AdcVolumeSet | Volume control of analog-to-digital converter |

**3.2.2 ALC**

The analog-to-digital converter contains a hardware automatic gain control unit inside, and the ALC is used to continuously control the signal amplitude of the PGA input.

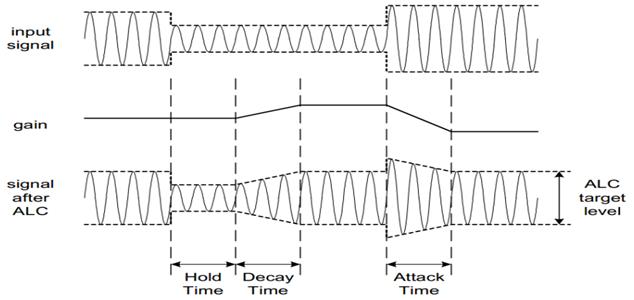


Figure 5 Schematic diagram of ALC

Table 3 ALC-related Functions

|  |  |
| --- | --- |
| Function name | Description |
| AdcAlcTimeConfig | Configure ALC-related parameters and enable the ALC function |
| AdcAlcTargetLevelConfig |
| AdcAlcSel |
| AdcAlcConfig | Similar to the above three function combinations, the difference lies in that this function sets the hold time to 0 |
| AdcAlcNoiseGateSet | The noise threshold value and the type of noise processing Settings |
| AdcAlcGainSet | Set the maximum and minimum gain values of the ALC |

**3.2.3 Output Type**

After the analog audio data signal undergoes volume control and mixing by the PGA and processing by the analog-to-digital converter, it is ultimately converted into digital sampling values and handed over to the subsequent digital circuit. The Audio ADC supports two output types: one is to only save to the PMEM memory, and the other is to write to the I2S circuit simultaneously when writing to the PMEM memory.

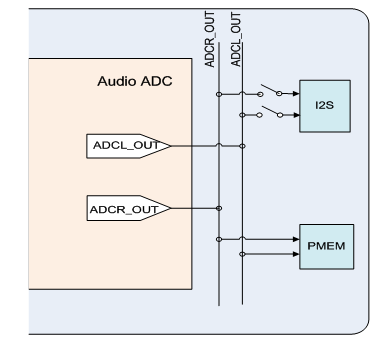


Figure 6 Output Type Selection Diagram

Table 4 Output type-related functions

|  |  |
| --- | --- |
| Function name | Description |
| AdcConfig | 1. Configure to write only to PMEM |
| AdcToPmem |
| AdcToI2s | 2. If this function is configured after 1, it will not only be written to the PMEM but also to the I2S circuit. |
| AdcPmemWriteEn | 3. Enable or pause data writing to PMEM |
| AdcPmemWriteDis |

**3.3 Clock Mode**

The AUDIO ADC shares the same master clock source with the DAC and I2S. Its source supports two types: one can be generated by an internal generator, and the other is injected into an external clock through GPIO.

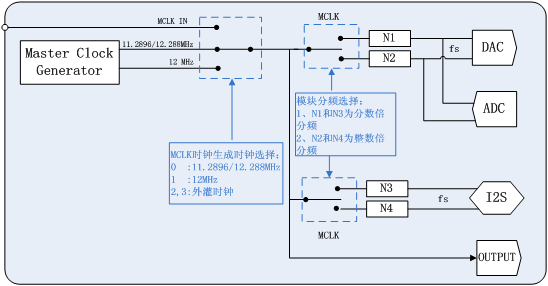


Figure 7 Clock Mode Block Diagram

Translation:

MCLK时钟生成时钟选择：= MCLK clock generation clock selection:

0 :11.2896/12.288MHz

1 :12MHz

2,3:外灌时钟= 2, 3: External injection clock

Translation:

模块分频选择：= Module frequency division selection:

I. NI和N3为分数倍= I. NI and N3 are fractional multiples

分频=Frequency division

2、N2和N4为整数倍=2. N2 and N4 are integer multiples

分频=Frequency division

**3.3.1 Audio Clock Relationship**

As shown in the following figure, the Audio ADC clock can come from the internal generator or from the external injection clock. Among them, the internal generator can output two different types of clocks, namely the NORMAL MODE and USB MODE usually defined in the SDK. The main clock of NORMAL MODE is an integer multiple of the sampling rate, that is, MCLK = N \* fs, where fs is the sampling rate and N is a positive integer. The USB MODE is not affected by the sampling rate and has a fixed output of 12MHz.

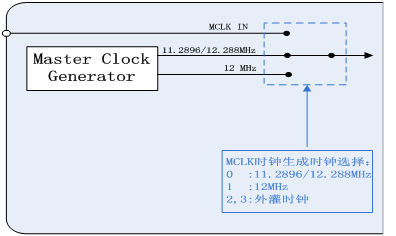


Figure 8 MCLK Clock Block Diagram

Translation:

MCLK时钟生成时钟选择：= MCLK clock generation clock selection:

0 :11.2896/12.288MHz

1 :12MHz

2,3:外灌时钟= 2, 3: External injection clock

The functions involved in the selection of the master clock source in the Audio ADC module are shown in the following table:

Table 5 Relevant functions for Selecting the main clock Source of the Audio ADC module

|  |  |
| --- | --- |
| Function name | Description |
| DacAdcSampleRateSet | The Mode parameter in the function interface is the selection of the main clock source: 12MHz, 11.2896/12.288MHz or an external clock |
| Adc8KDac48KSampleRateSet |
| Adc48KDac8KSampleRateSet |

**3.3.2 Sampling Rate and Master Clock**

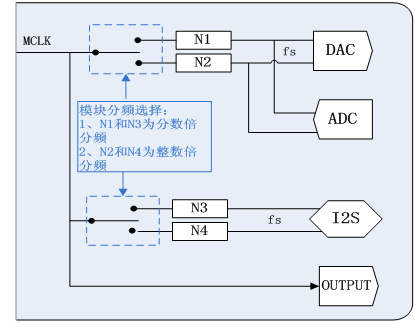


Figure 9 Relationship Between Master Clock and fs

Translation:

模块分频选择：= Module frequency division selection:

I. NI和N3为分数倍= I. NI and N3 are fractional multiples

分频=Frequency division

2、N2和N4为整数倍=2. N2 and N4 are integer multiples

分频=Frequency division

As shown in Figure 6, the sampling division ratio of the Audio ADC supports two types, namely N1 and N2. Among them, N1 is the fractional multiple relationship of the sampling rate and is applicable to the 12MHz master clock. N2 is an integer multiple of the sampling rate and is applicable to 11.2896/12.288MHz. Therefore, the frequency division ratio of the sampling rate of the Audio ADC must be consistent with the type of the master clock; otherwise, the obtained sampling rate will be different from the theoretical value.

Table 6 Relevant functions for setting the audio ADC crossover ratio

|  |  |
| --- | --- |
| Function name | Description |
| AdcConfig | The ClkMode in the function interface refers to the selection of the frequency division ratio for the Audio ADC sampling rate |
| AdcToPmem |
| AdcToI2s |
| AdcDacClkModeSet |

**3.3.3 Fine-tuning mechanism**

The Audio ADC supports two mechanisms: hardware fine-tuning and software fine-tuning. The hardware fine-tuning mechanism is only applicable to USB MODE. The software fine-tuning mechanism is applicable in both clock modes, but it is recommended to use the hardware fine-tuning mechanism in USB MODE.

Table 7 Scope of application of fine-tuning mechanism

|  |  |  |
| --- | --- | --- |
| Fine-tuning mechanism | USB MODE | NORMAL MODE |
| Hardware fine-tuning mechanism | √ | × |
| Software fine-tuning mechanism | √ | √ |

**4 Configuration Process**

Start configuration

Audio ADC

power-on initialization

Configure the PGA end

1. Input the audio source

2. Channel volume

Configure the ADC end

1.Configure PMEM

2. Configure output

3. Digital volume

4. Sampling frequency

Is ALC used?

Y

N

Configure and enable ALC

Configuration completed

Figure 10: Audio ADC Configuration Flow